



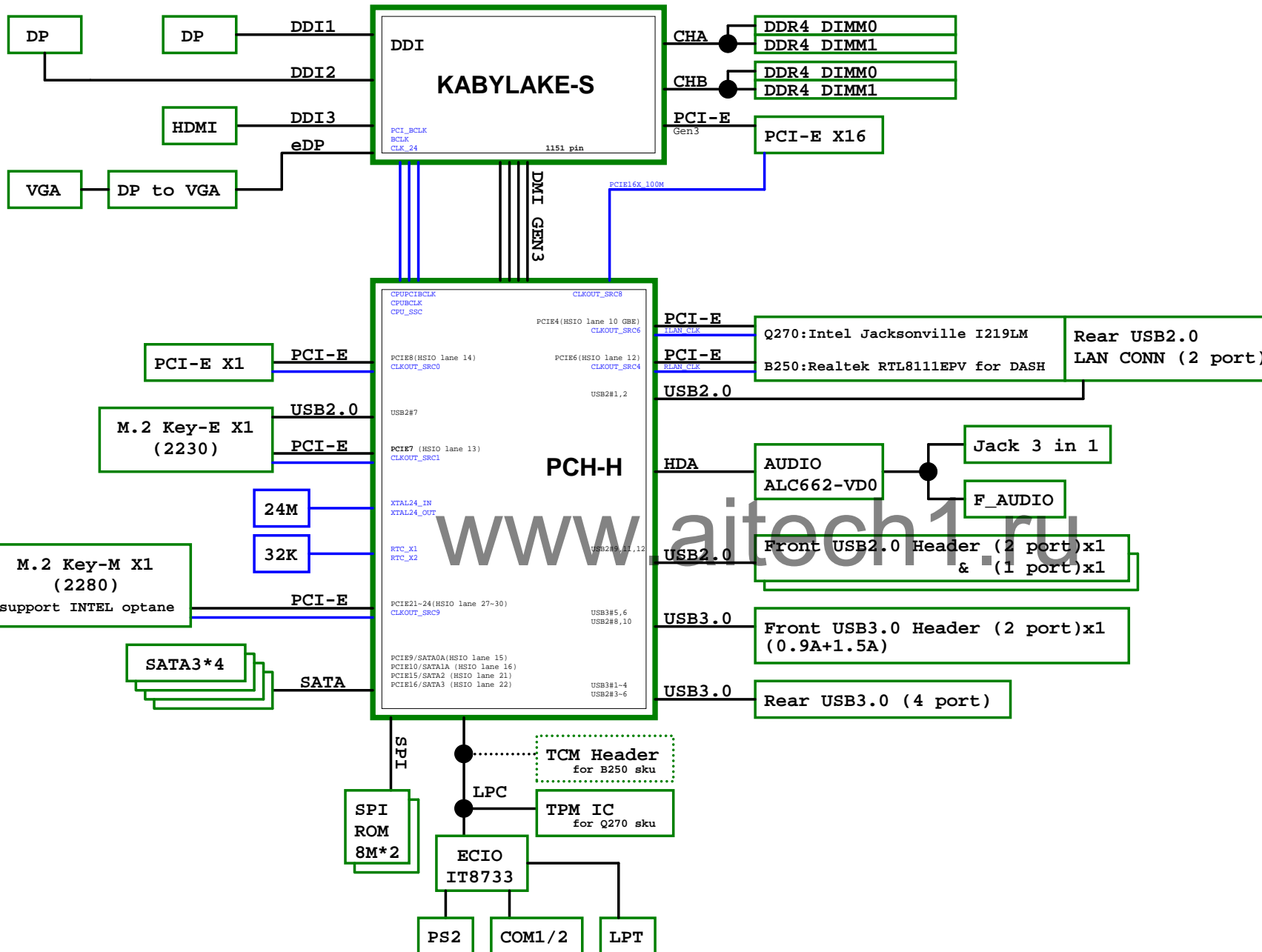
Q27H4-AD

Rev:1.0

ECS
CONFIDENTIAL

TABLE OF CONTENTS

Page	Index	Page	Index
1	Cover Page	28	FAN/PS2/Buzzer/F_Panel
2	Block Diagram	29	LPT/COM/TPM
3	GPIO Function & INT# Mapping	30	ECIO-IT8733
4	CPU-PEG/DMI/DDI	31	LAN I219LM/RTL8111EVP
5	CPU-MISC	32	USB2.0_LAN Connector
6	CPU-DDR4	33	AUDIO-ALC662_VD
7	CPU-POWER	34	AUDIO-CONN & Header
8	CPU-GND	35	SEQUENCE circuit
9	DDR4-CHA	36	ATX POWER/EuP circuit
10	DDR4-CHB	37	DC/DC +VCC/+VCC3
11	DDR4-Vref	38	DC/DC +VDIMM+DDR_VTT
12	PCIE*16/PCIE*1	39	DC/DC +V1P0A /+5VDUAL_1P0A
13	reserved	40	DC/DC +VCCIO
14	DP1/DP2	41	DC/DC +VCORE PWM IC
15	HDMI	42	DC/DC +VCORE DRIVER IC
16	VGA (RTD2166)	43	DC/DC +VCCGT/+VSA
17	PCH-MISC	44	PWR Delivery
18	PCH-DMI/USB2.0/PCIE[1:8]	45	PWR Sequence
19	PCH-USB3.0/CLK/LPC	46	History
20	PCH-SATA/HOST/PCIE[9:20]	47	reserved
21	PCH-POWER		
22	PCH-GND/GPIO		
23	USB2.0 Header		
24	USB3.0 Header		
25	USB2.0*4 Connector		
26	M.2 WLAN/SSD		
27	SPI/SMbus/BIOS_WP		



PCH-GPIO function

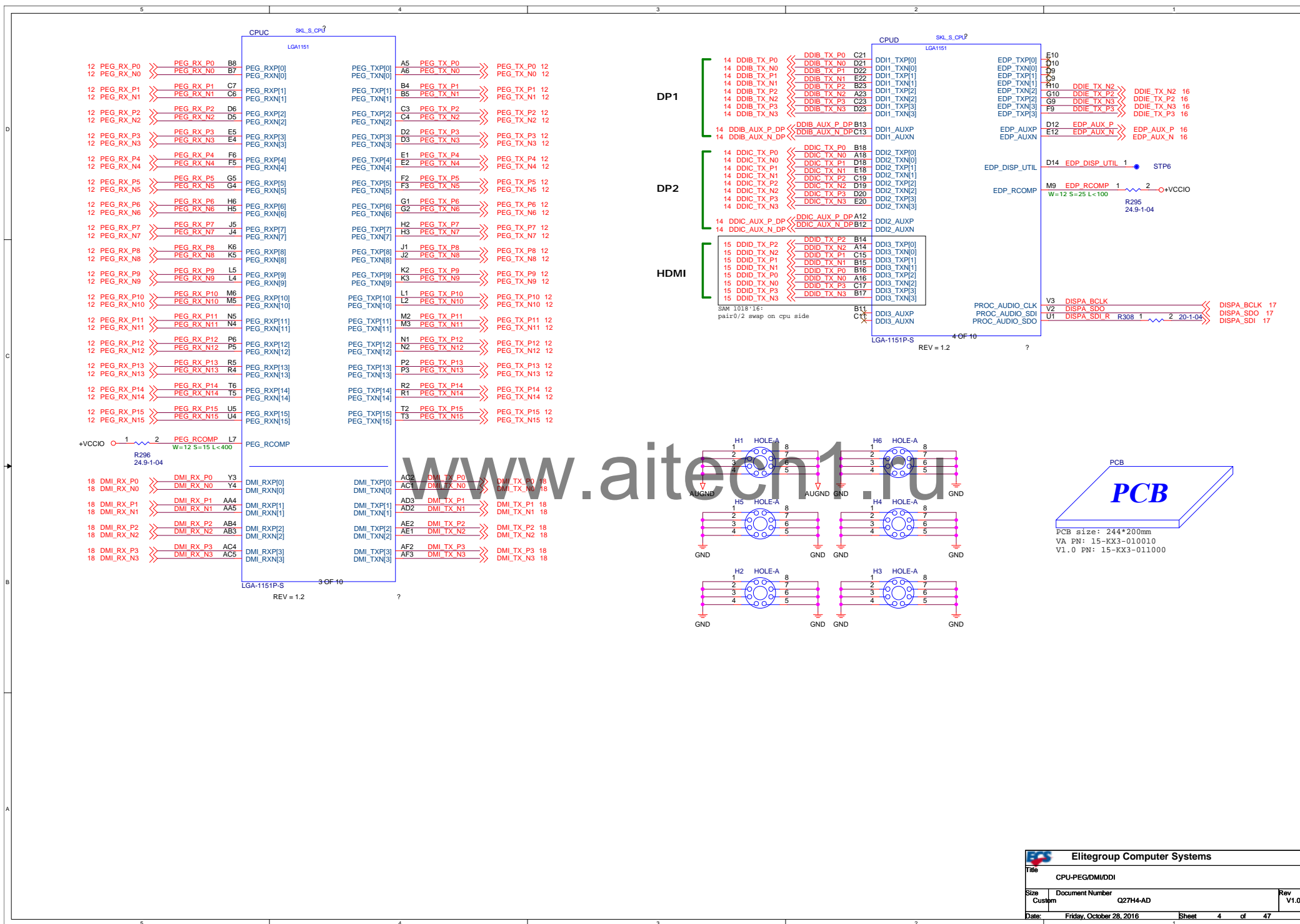
Pin Name	Power Well	Usage	Default Status
GPP_D7	3VSB	GPP_D7_CASEOPEN (reserved)	GPIO(GPI)
GPP_D6	3VSB	GPP_D6_BIOSWP	GPIO(GPI)
GPP_D5	3VSB	GPP_D5_BIOS_WP	GPIO(GPI)
GPD10	ATX_3VSB	GPD10 (ME disable by SW)	SLP_S5#
GPD2	ATX_3VSB	ILAN_WAKE_L	LAN_WAKE#
GPD0	ATX_3VSB	RLAN_PWR_EN (only for B25 sku)	BATLOW#
GPD11	ATX_3VSB	LAN_DIS_L	LANPHYPC
GPP_A12	3VSB	GPP_A12_TPM H:with on-board TPM L:W/O on-board TPM	GPIO(GPI)
GPP_A11	3VSB	LPC_PME_L	PME#
GPP_G13	VCC3	HDPANEL_DETECT (reserved)	GPIO(GPI)
GPP_A14	VCC3	LPCPD_L	SUS_STAT#
GPP_A0	VCC3	KBRST_L_RC	RCIN#
GPP_A6	VCC3	SERIRQ	SERIRQ
GPP_A5	N/A	LPC_FRAME_L	LFRAME#
GPP_A1	N/A	LPC_LAD0	LAD0
GPP_A2	N/A	LPC_LAD1	LAD1
GPP_A3	N/A	LPC_LAD2	LAD2
GPP_A4	N/A	LPC_LAD3	LAD3
GPP_A9	N/A	PCH_SIO_24M	CLKOUT_LPC0
GPP_A10	N/A	TCM_TPM_24M	CLKOUT_LPC1
GPP_B3	VCC3	BT_DISABLE_L L:disable	GPIO(GPI)
GPP_B17	VCC3	WLAN_DISABLE_L L:disable	GPIO(GPI)
GPP_E8	VCC3	SATALED_L	SATA_LED#
GPP_F16	3VSB	GPP_F16 H: USB power enable	GPIO(GPI)
GPP_I0	N/A	DDPB_HPD0	DDPB_HPD0
GPP_I1	N/A	DDPC_HPD1	DDPC_HPD1
GPP_I2	N/A	DDPD_HPD2	DDPD_HPD2
GPP_I2	N/A	DDPE_HPD3	DDPE_HPD3
GPP_G23	3VSB	GPP_G22 H:default BIOS L:on-board VGA	GPIO(GPI)
GPP_F22	VCC3	GPP_F22_PCIEIRST (PCIEx16 SW RST#)	GPIO(GPI)
GPD9	ATX_3VSB	PCH_RI_L L:RI# wake up	SLP_WLAN#
GPP_H0	3VSB	ILAN_CLKREQ	SRCCCLKREQ6#
GPP_B6	3VSB	M2CLK_REQ1_L	SRCCCLKREQ1#
GPP_E0	3VSB	GPP_E0_OBR (ACER's OBR)	GPIO(GPI)
GPP_H14	3VSB	GPP_H14 (ACER reserved GPIO)	GPIO(GPI)
GPP_H15	3VSB	GPP_H15 (ACER reserved GPIO)	GPIO(GPI)
GPP_D1	+DIMM_5VDUAL	SIO_LED1	GPIO(GPI)
GPP_D0	+DIMM_5VDUAL	SIO_LED0	GPIO(GPI)

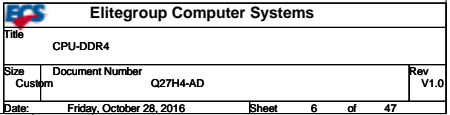
SIO-GPIO function

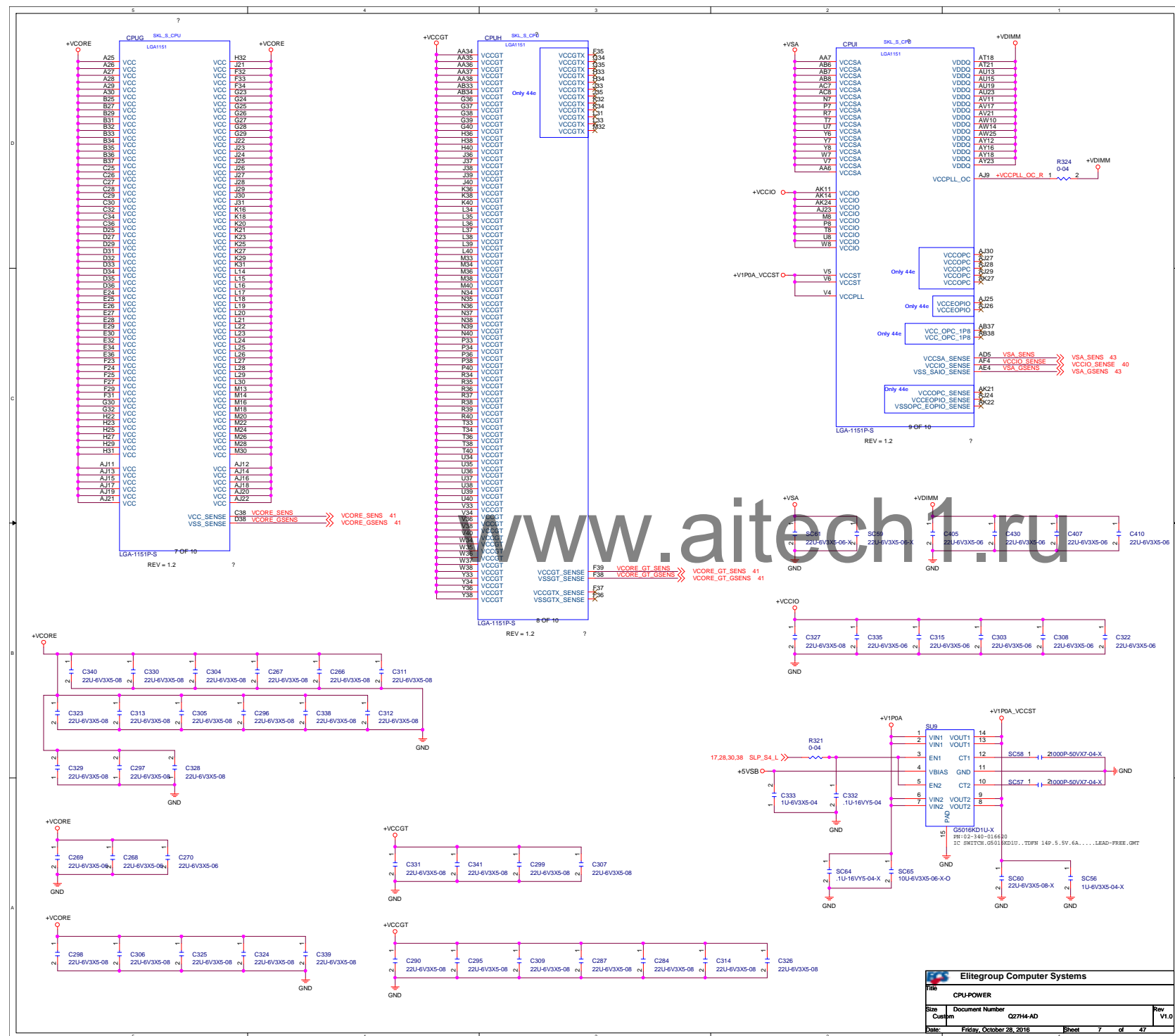
Pin Name	Power Well	Usage	Default Status
GP16	3VSB	basic health function	5VSB_CTRL#(DOD8)
GP31	3VSB	EC sleep mode wake up	PWNOUT(DOD8)
GP41	3VSB	GPP_E7_THERM (ACER's SW thermal shutdown)	FAN_CTL3(DOD8)
GP17,GP35	3VSB	VGA Wake up by Monitor (EC control)	
GP36,GP37	3VSB	HDMI Wake up by Monitor (EC control)	
GP34	3VSB	DP2 Wake up by Monitor (EC control)	
GP33	3VSB	DP1 Wake up by Monitor (EC control)	

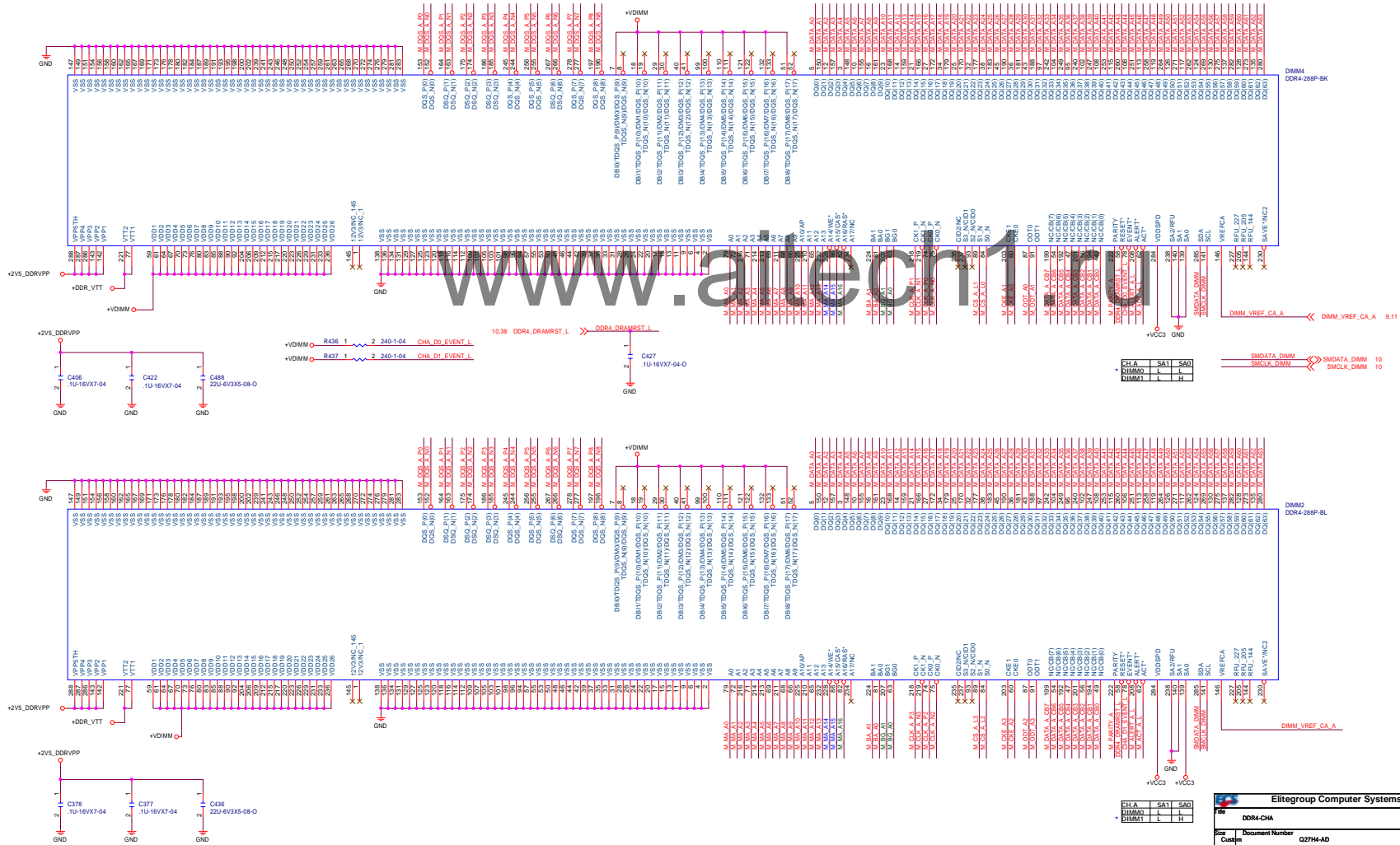
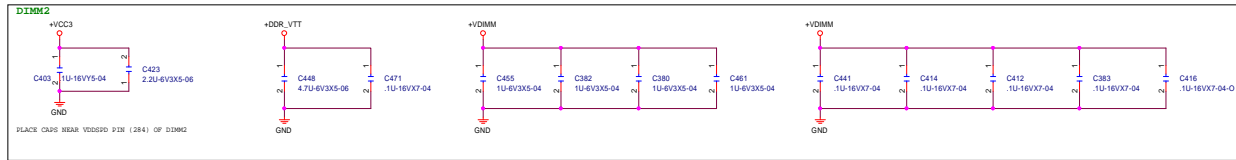
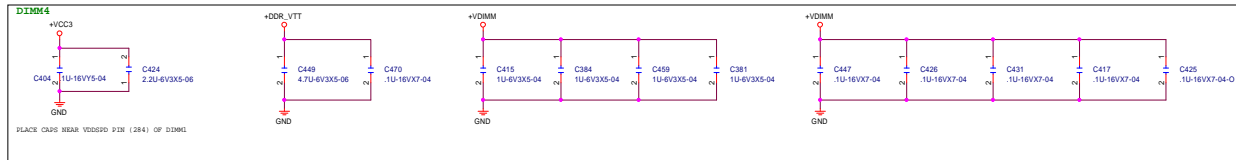
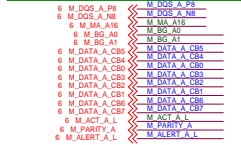
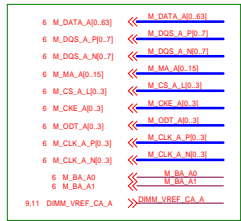
CPU-Strap

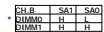
Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted CFG[1]: Reserved configuration lane	1 = (Default) Normal Operation
CFG1		
CFG2:5/6	CFG[2]: 1 = Normal operation CFG[6:5]: 1 = 1 x16 PCI Express CFG[3]: Reserved configuration lane.	PCIEX6X
CFG3		
CFG4	CFG[4]: eDP enable:	0 = Enable
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lines.	
SPKR/GPP_B14	Top Swap Override	0 = Enable "Top Swap" mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 = Enable "No Reboot" mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit HBS	0 = SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 = LPC is selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPD_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.



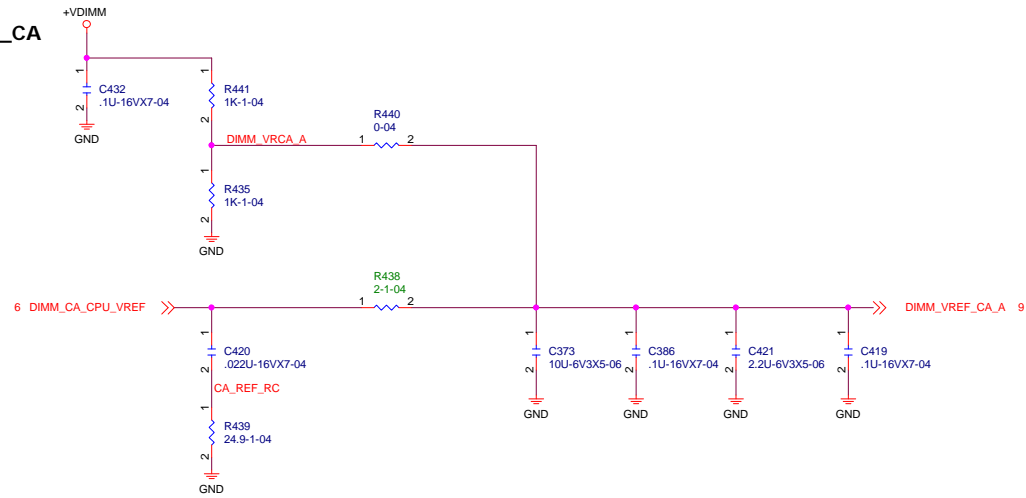




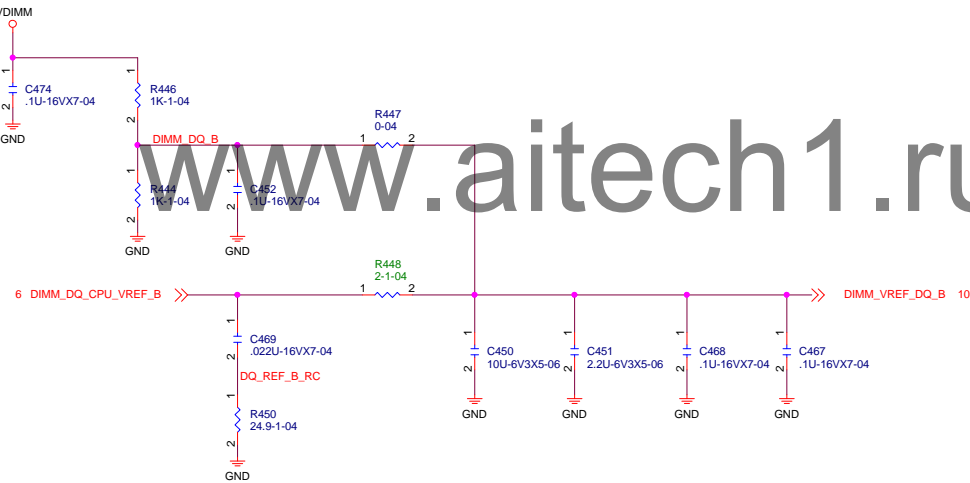




DIMM_VREF_CA




DIMM_VREF_DQ

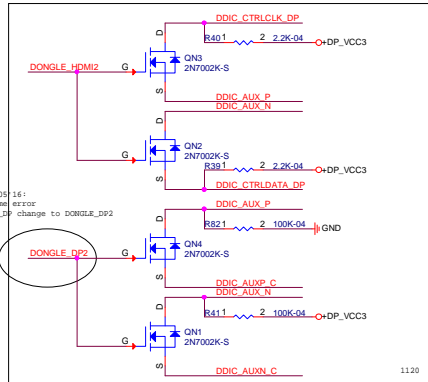
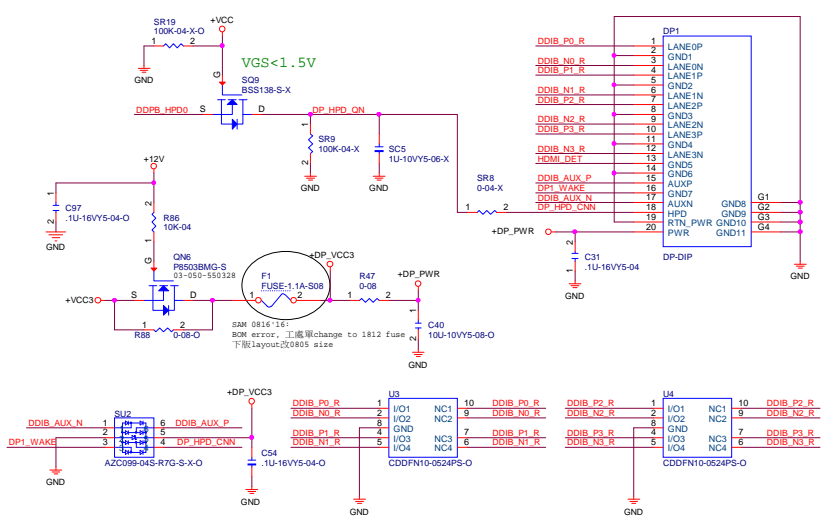
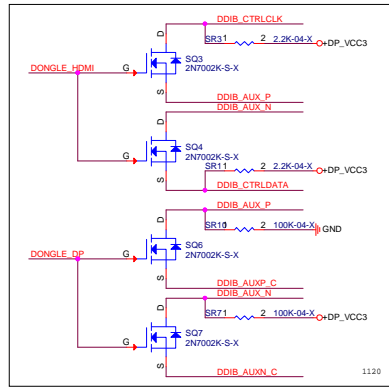


Elitegroup Computer Systems			
Title	DDR4-Vref		
Size	Custom	Document Number	Q27H4-AD
Date:	Friday, October 28, 2016	Sheet	11 of 47
Rev	V1.0		

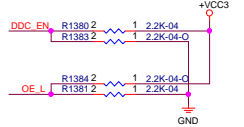
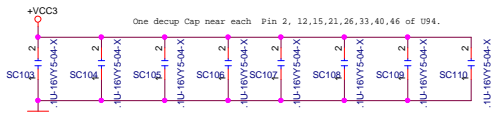
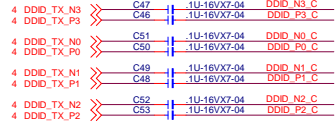
www.aitech1.ru

 Elitegroup Computer Systems	
Title reserved	
Size Custom	Document Number Q27H4-AD
Date: Friday, October 28, 2016	Rev V1.0
Sheet 13 of 47	

DP1
DP2

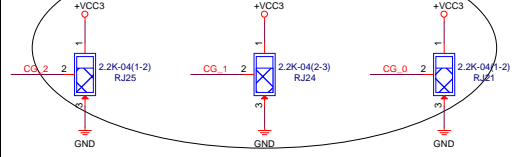


HDMI

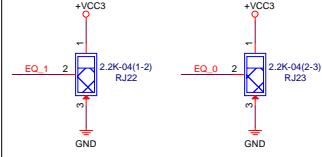


Sam 1205'16
C00,1,2=1:0:1 for SI eye & VL

CG0=1,CG1=0,CG2=1



EQ1=1, EQ0=0

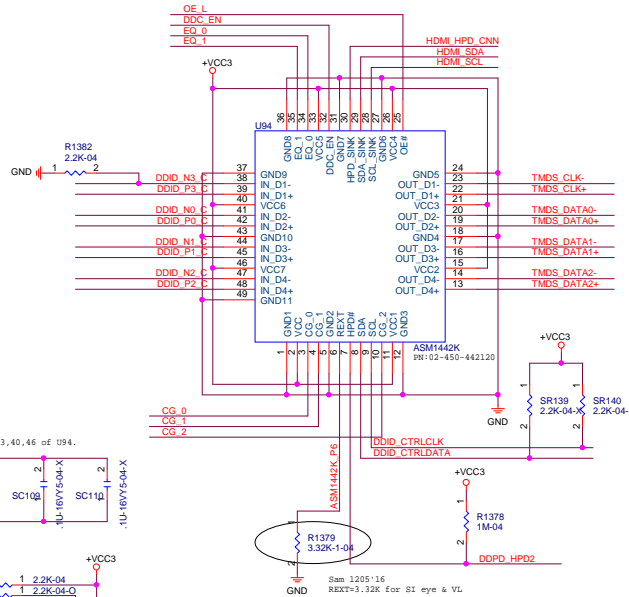


TMDS Input Signal Equalization

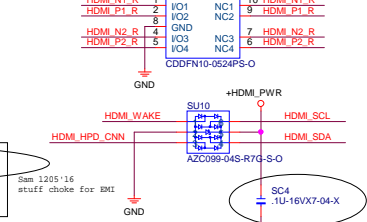
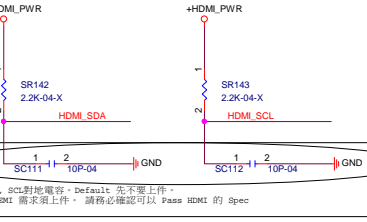
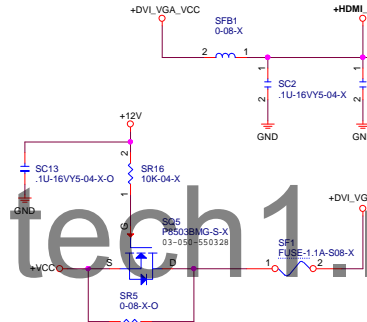
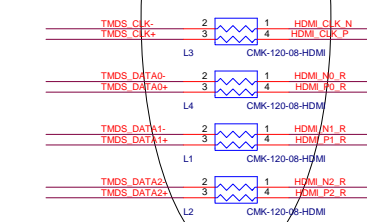
EQ_1	EQ_0	Equalization	Note
0	0	6dB	
0	1	3dB	
1	0	1dB	default
1	1	0dB	

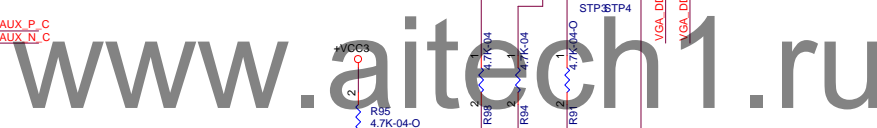
TMDS Output Signal Integrity

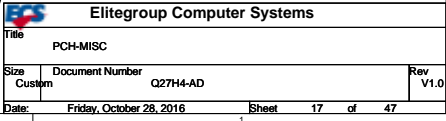
CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note
0	0	0	453	0	0	
0	0	1	458	0	-0.86dB	
0	1	0	461	0	-1.64dB	Default
0	1	1	465	0	-0.86dB	
1	0	0	473	0	-1.64dB	
1	0	1	430	0.3dB	0	
1	1	0	425	0.3dB	0	
1	1	1	455	0	0	

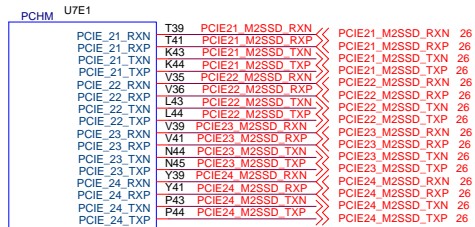


Sam 1205'16
stuff choke for EMI

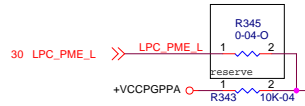




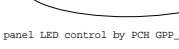
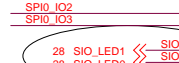




KBL_PCH_HBGA
REV#0.7



integrated Pull up 15K-40K



SAM 1021:16:
change front panel LED control by PCH GPP_D0/D1

PCBA

GPP_A11/PME#

RSVD_18

RSVD_19

RSVD_20

RSVD_21

AU19

AP17

TP2

TP1

SPI0_MOSI

SPI0_MISO

SPI0_CS0#

SPI0_CLK

SPI0_CS1#

SPI0_IO2

SPI0_IO3

SPI0_CS#

GPP_D1/SPH1_CLK

GPP_D0/SPH1_CS#

GPP_D3/SPH1_MOSI

GPP_D2/SPH1_MISO

GPP_D22/SPH1_IO3

GPP_D21/SPH1_IO2

INTRUDER#

GPP_B13/PLTRST#

GPP_G16/GSXCLK

GPP_G12/GSXDOU

GPP_G13/GSXSLD

GPP_G14/GSXSDIN

GPP_G15/GSXRESET#

GPP_E3/CPU_GP0

GPP_E7/CPU_GP1

GPP_B3/CPU_GP2

GPP_B4/CPU_GP3

GPP_H18/SML4ALERT#

GPP_H16/SML4CLK

GPP_H15/SML3ALERT#

GPP_H14/SML3DATA

GPP_H13/SML3CLK

GPP_H12/SML2ALERT#

GPP_H11/SML2DATA

GPP_H10/SML2CLK

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

GPP_H14

GPP_H13

GPP_H12

GPP_H11

GPP_H10

GPP_H18

GPP_H15

GPP_H12

GPP_H17

GPP_H16

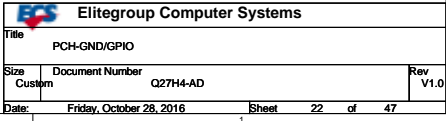
GPP_H14

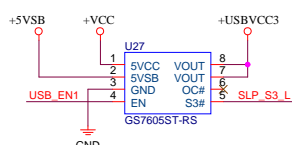
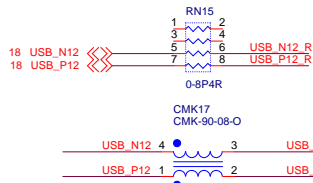
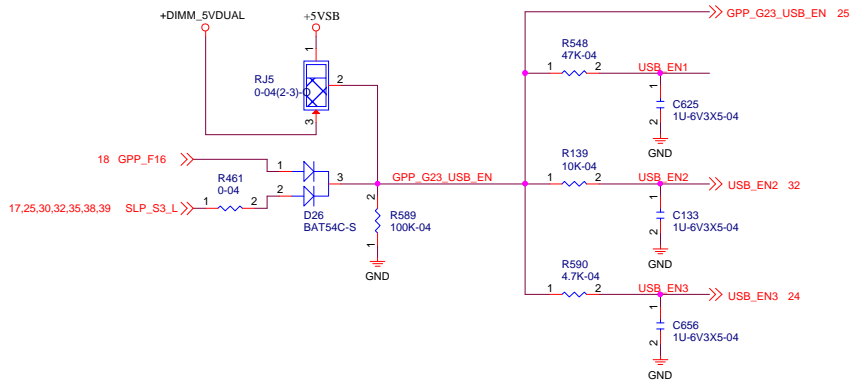
GPP_H13

GPP_H12

GPP_H11

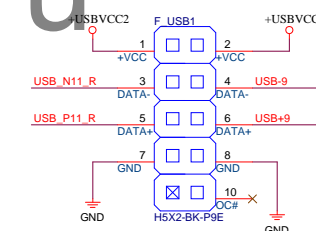
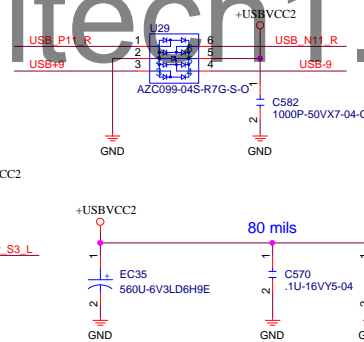
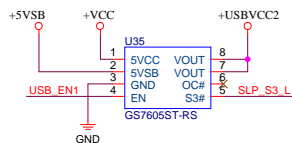
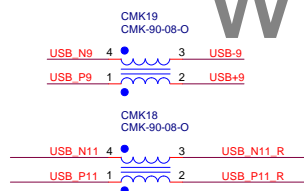
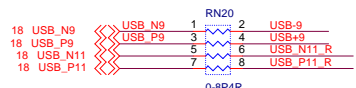
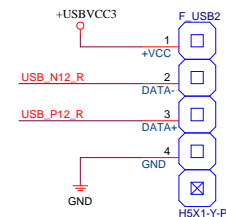
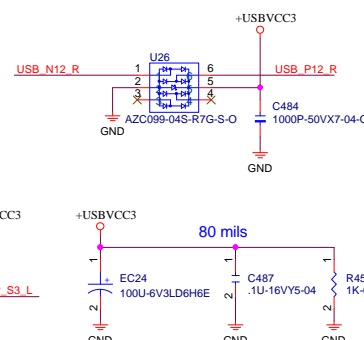
GPP_H10



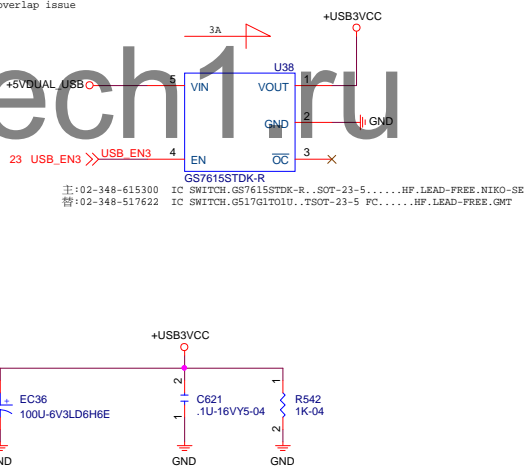
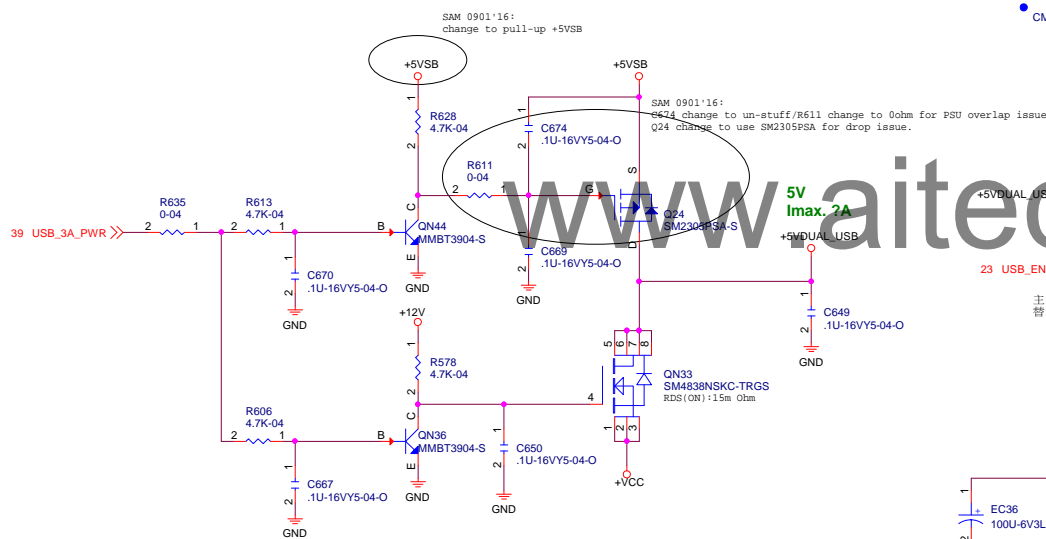
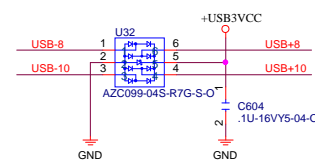
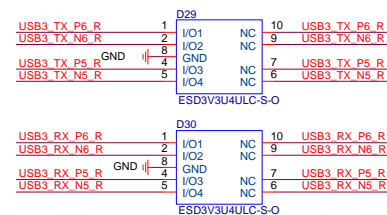
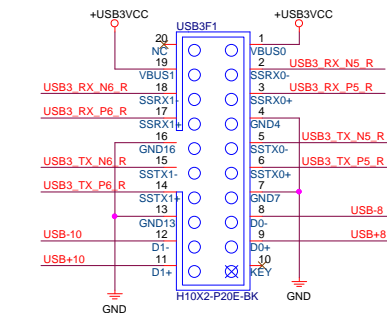
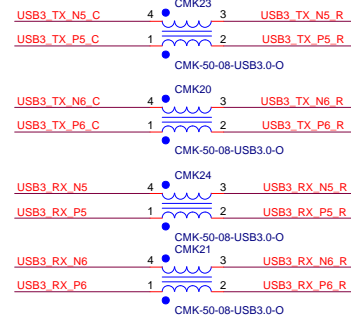
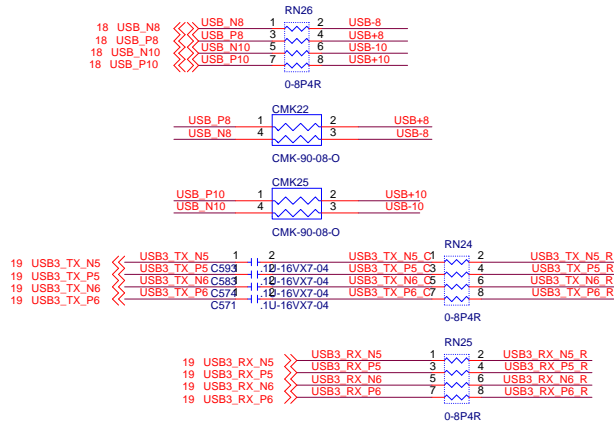


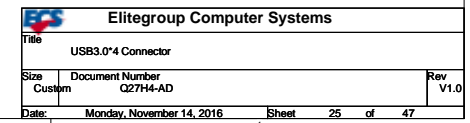
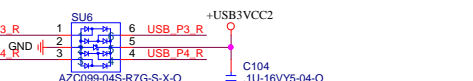
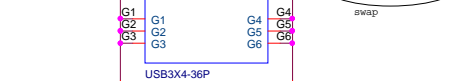
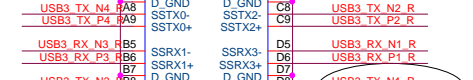
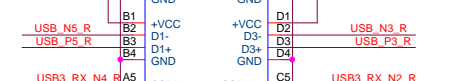
	power switch Enable use	RJ5	D62	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 W S5 W/O USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	Stuff	S4 : 5 Volt S5 : 0 Volt	

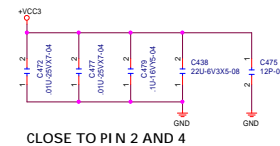
STATUS	S0	S3	S4	S5
GPP_F16	HI	HI	HI	LOW
USB_PWR	ON	ON	ON	OFF



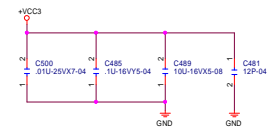
www.aitech1.ru



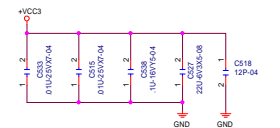


[illegible]

CLOSE TO PIN 2 AND 4



CLOSE TO PIN 12,14,16 AND 18



CLOSE TO PIN 70 72 AND 74

The schematic diagram illustrates the SMBus interface circuit. It shows the connection of +3VSB and +VCC3 to the SMBus lines (SMBCLK and SMBDATA) through resistors R638, R641, R636, and R639. The circuit includes a pull-up resistor R576 (1K-04) for the +3VSB line and a pull-down resistor R577 (4.7K-04) for the PCH_PWROK signal. The SMBus lines are connected to the QN42 and QN43 transistors, which are controlled by the ATX_PWRGD_3VSB_3 signal. The output of the transistors is connected to the SMBCLK_MAIN and SMBDATA_MAIN lines, which are also connected to the SMBCLK_STBY and SMBDATA_STBY lines. The circuit is powered by +12V and +3VSB, with ground connections for GND.

The diagram illustrates the SPI interface connections for two memory chips, SPIROM1 and SPIROM2, connected to an external memory. The connections are as follows:

- SPIROM1:**
 - SPI0_MOSI:** Connected to R539 (2) and R540 (1).
 - SPI0_MISO:** Connected to R538 (2) and R540 (1).
 - SPI0_CLK:** Connected to R534 (2) and R535 (1).
 - SPI_CS_L0:** Connected to R521 (1) and R524 (0-04).
 - SPI_CS_L1:** Connected to R521 (1) and R524 (0-04).
- SPIROM2:**
 - SPI0_MOSI:** Connected to R527 (2) and R531 (1).
 - SPI0_MISO:** Connected to R527 (2) and R531 (1).
 - SPI0_CLK:** Connected to R527 (2) and R531 (1).
 - SPI_CS_L1:** Connected to R527 (2) and R531 (1).
 - SPI_CS_L0:** Connected to R527 (2) and R531 (1).

The diagram also shows the connection of SPI_CS_L0 and SPI_CS_L1 to the external memory. The diagram is labeled 'Re' and 'ROM1'.

BIOS_WP

JP-R(2-3)

H3X1-R

GND

BIOS_WP Jumper:

MODE	WP
BIOS_WP	1-2
NORMAL	2-3

* BIOS_WP

GPP_D6_BIOSWP 17

GPP_D5_BIOS_WP 17

SPI_WP

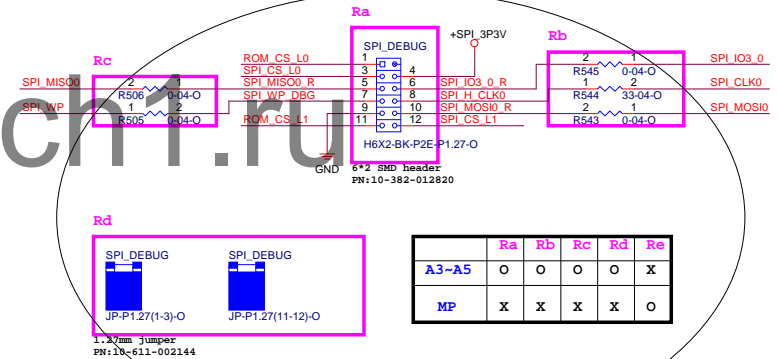
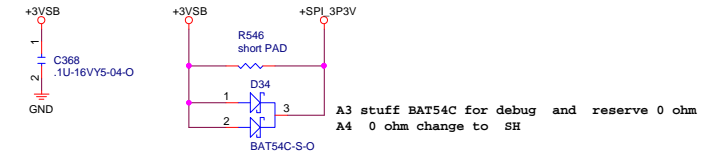
3P3V

R537 10K-04

R526 0-04

QP5 MMBT3906-S-O

GND



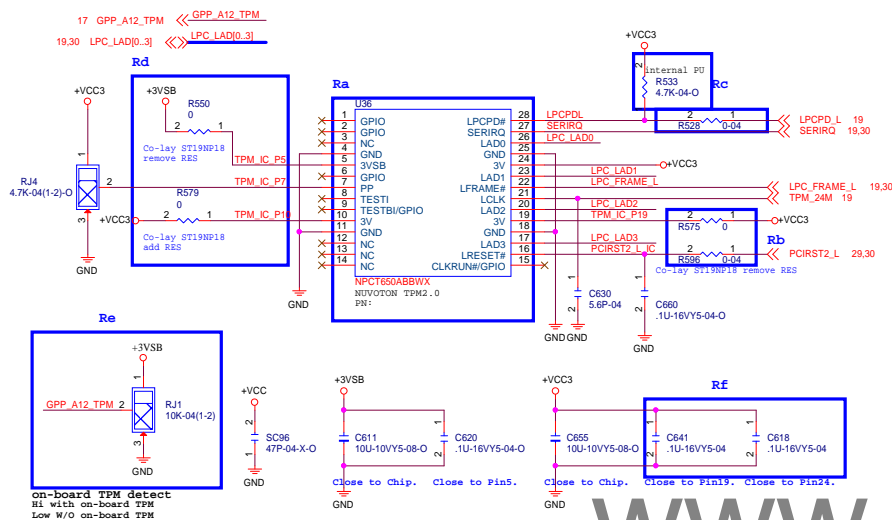
SAM 0901'16:
V1.0 SPI_DEBUG header不上件



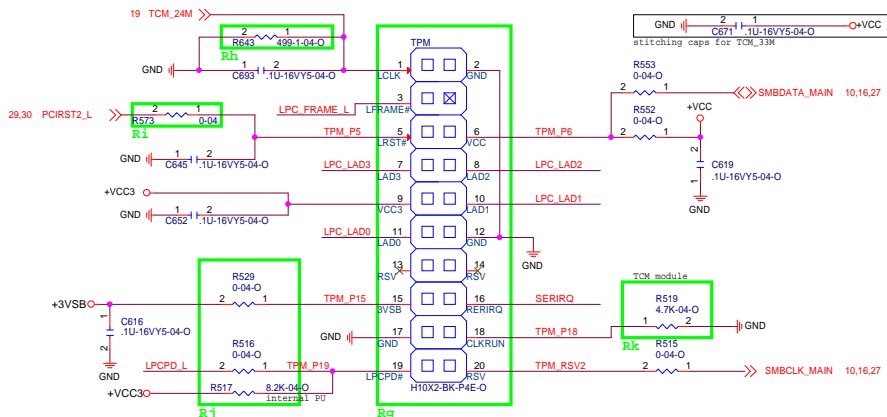
	normal	abnormal
S0	BLUE LED0=L LED1=H	RED blink LED0=blink LED1=L
S3	BLUE blink LED0=L LED1=blink	RED blink LED0=blink LED1=L

TPM chip/header circuit

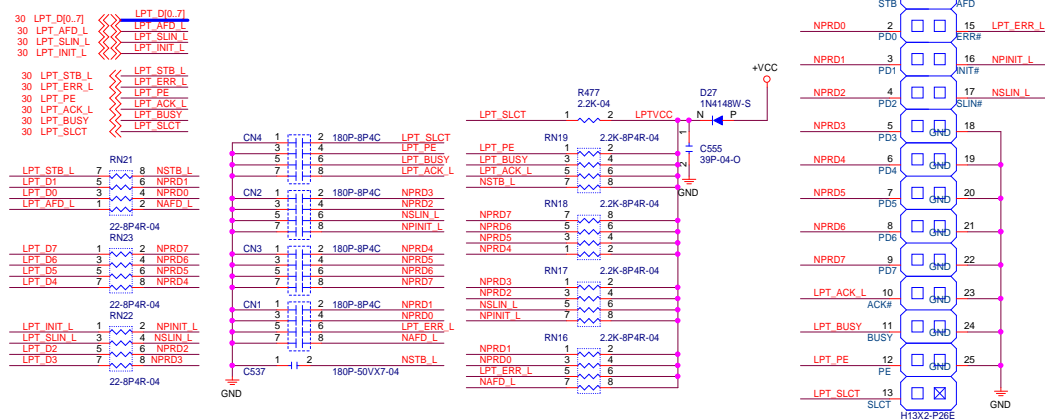
Ra-Rf IC										Rg-Rk Header										
Q170										Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri	Rj	Rk
for Acer										O	O	O	O	(1-2)	O	X	X	X	X	X
B150										Ra	Rb	Rc	Rd	Re	Rf	Rg	Rh	Ri	Rj	Rk
for Acer																				
Founder										X	X	X	X	(2-3)	X	O	O	O	O	O



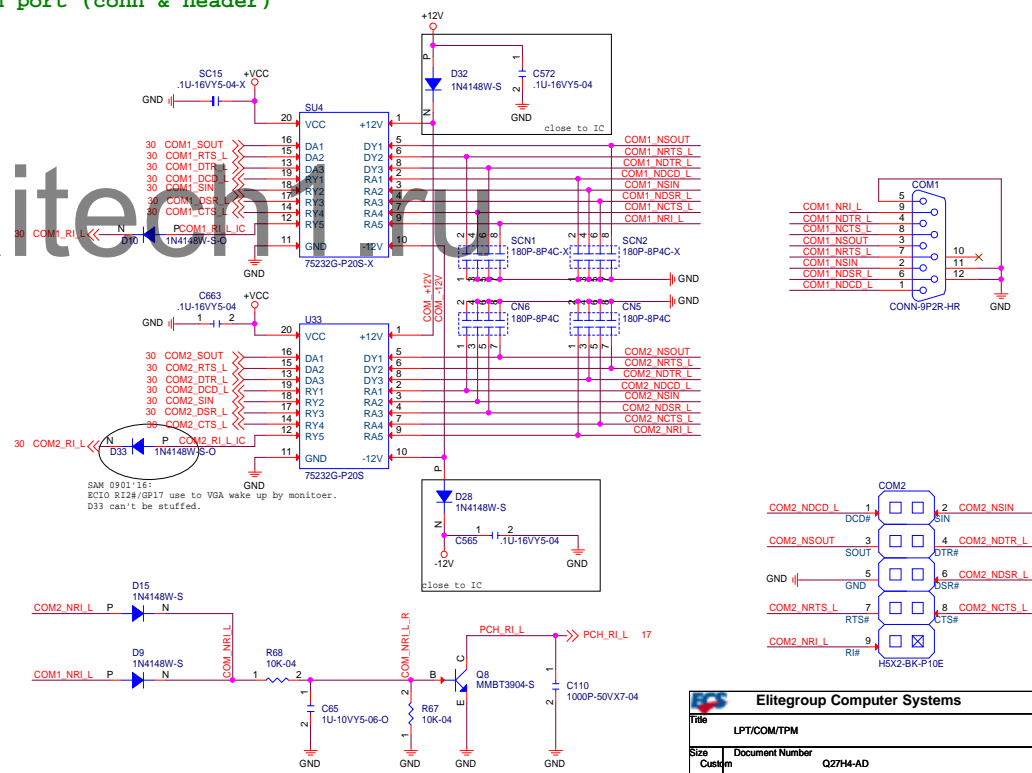
For B150

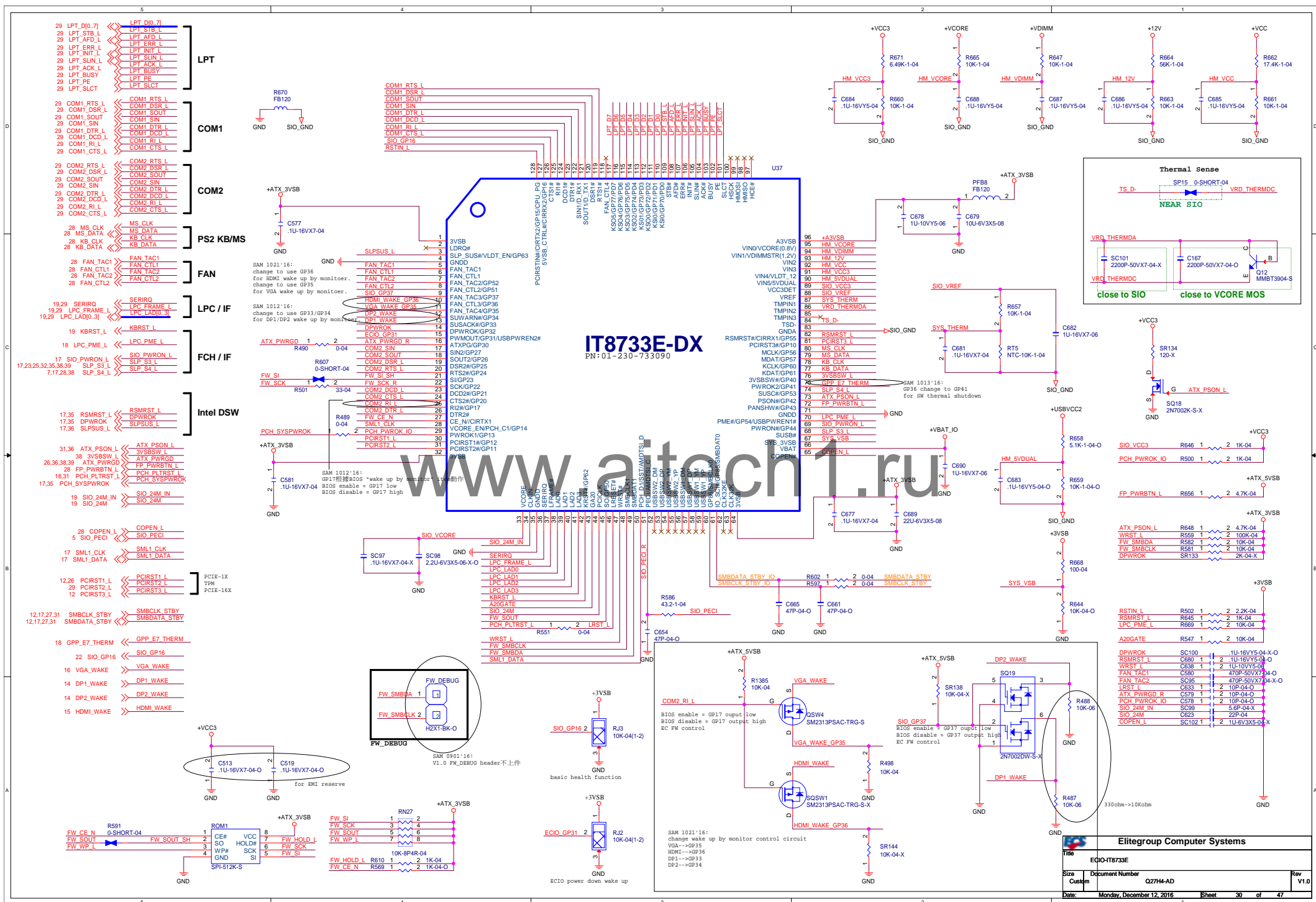


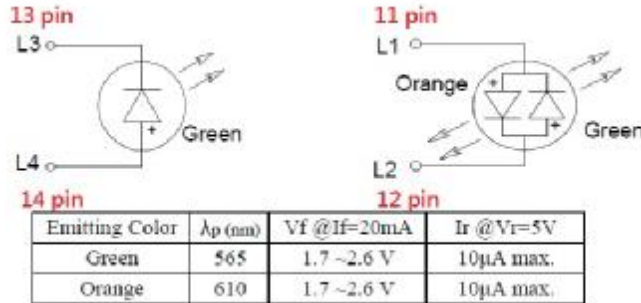
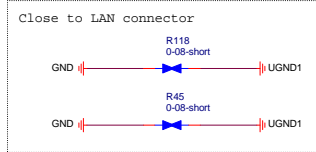
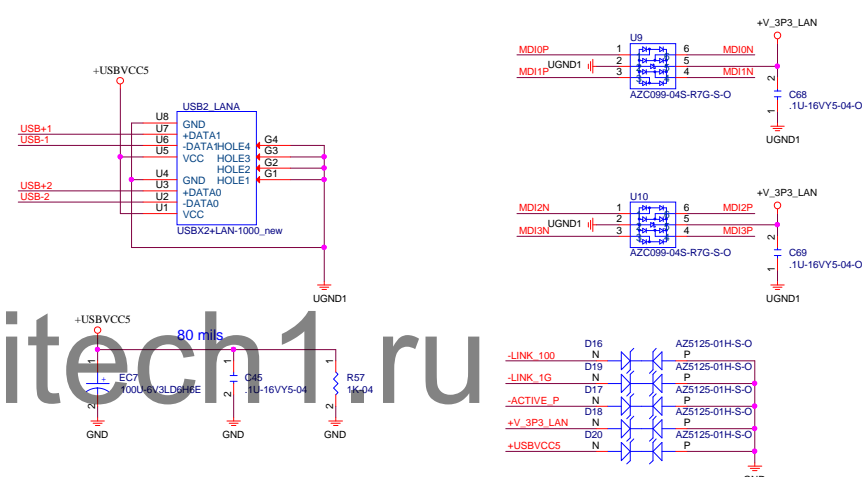
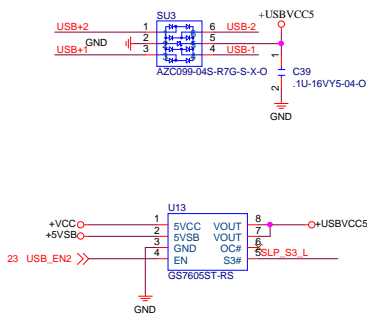
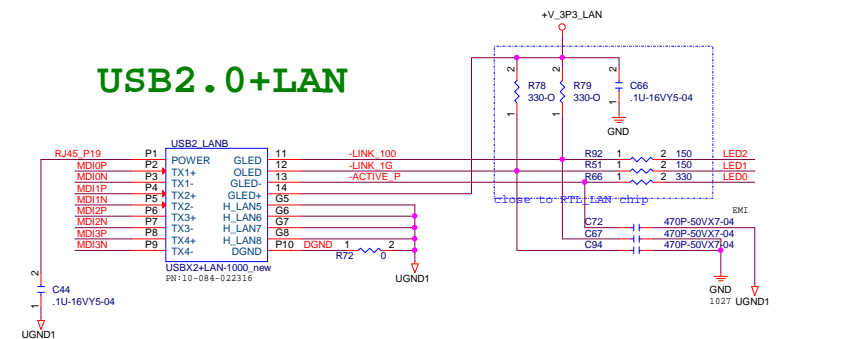
LPT Header



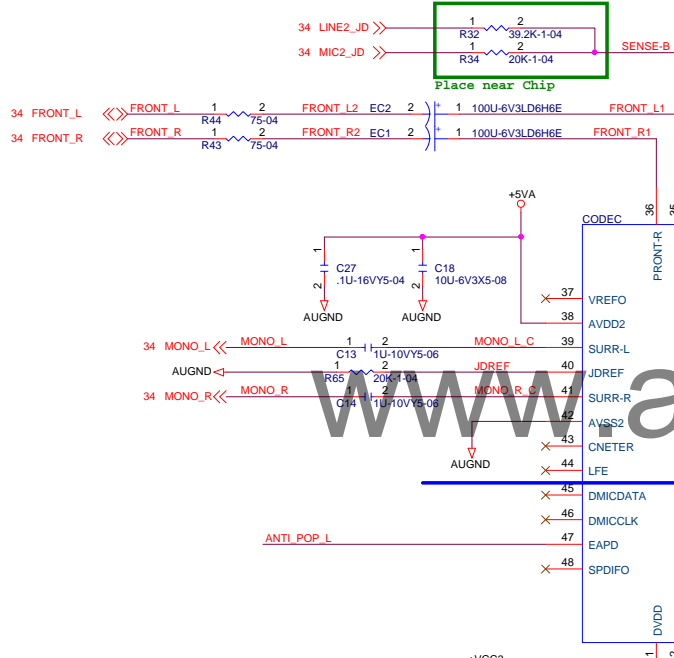
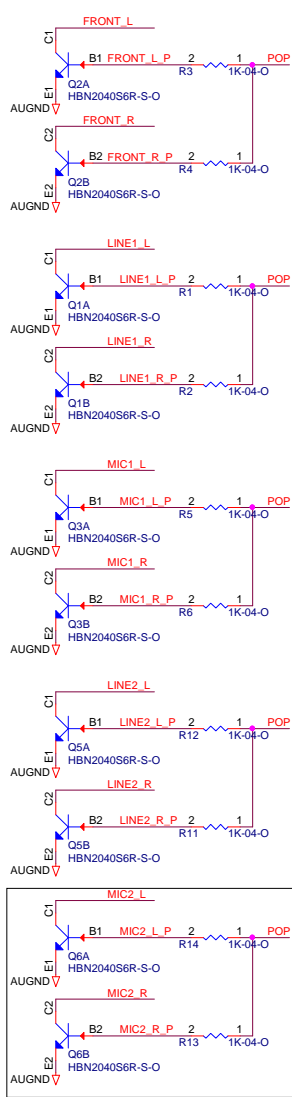
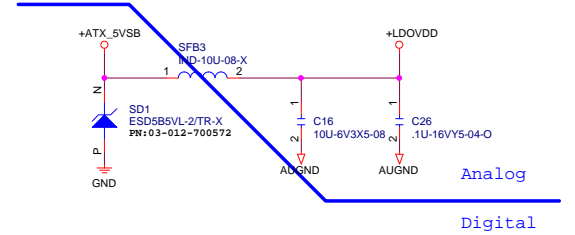
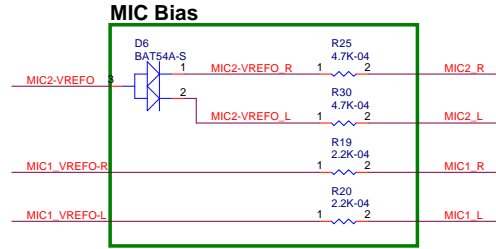
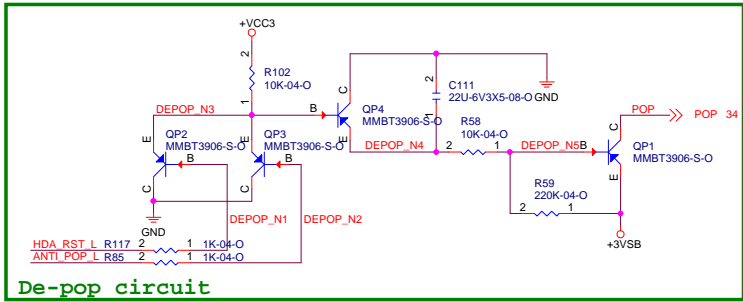
COM port (conn & header)



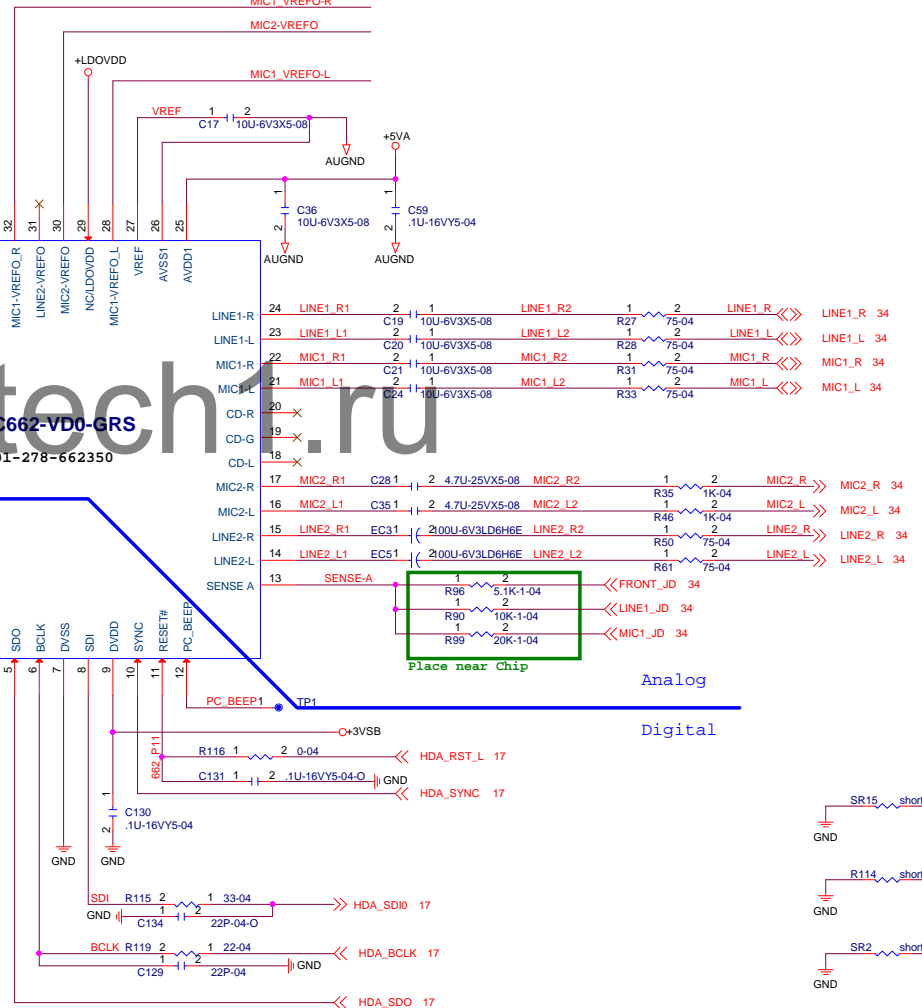




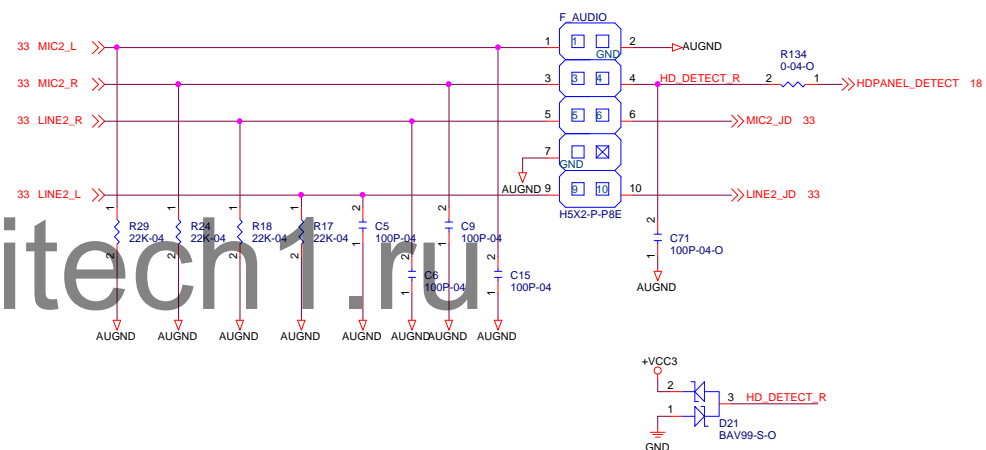
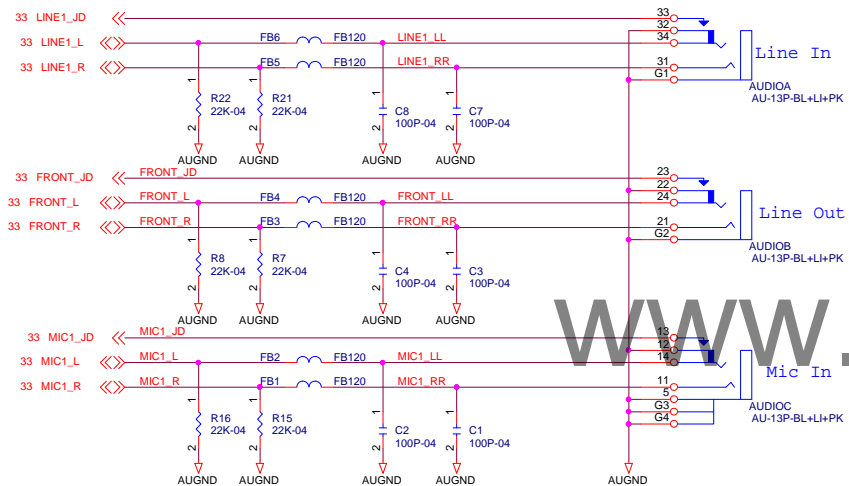
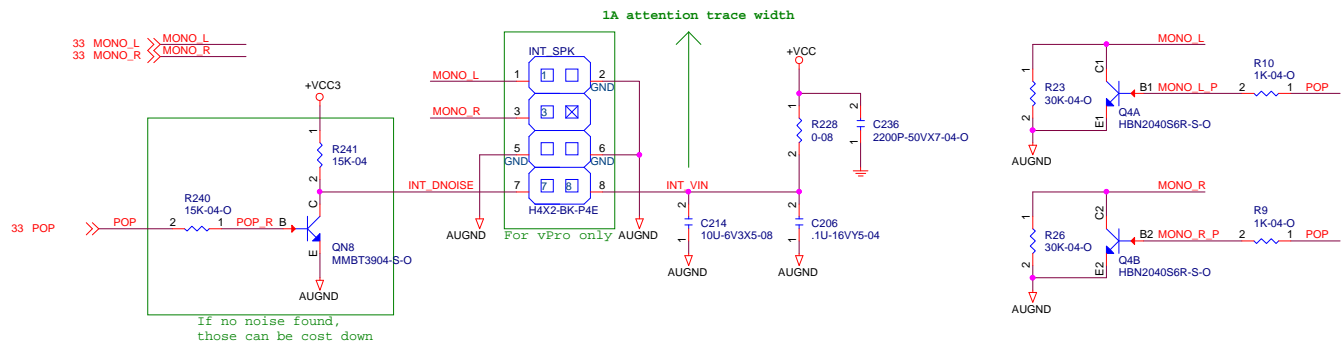
				S0	S3	S4	S5	G3 to S5
<div>Rear Side</div> <div><div>Active</div><div><div></div><div></div><div></div></div><div>Speed</div></div>	Active LED (Single Color)	Access	Blank	Blank	Blank	Blank		
		Not Access	OFF	OFF	OFF	OFF		
	Speed-LED (Dual Color)	Disconnected	OFF	OFF	OFF	OFF		
		100% ON with Amber Color	ON					
		100% ON with Green Color	ON					
1k: OFF		OFF						



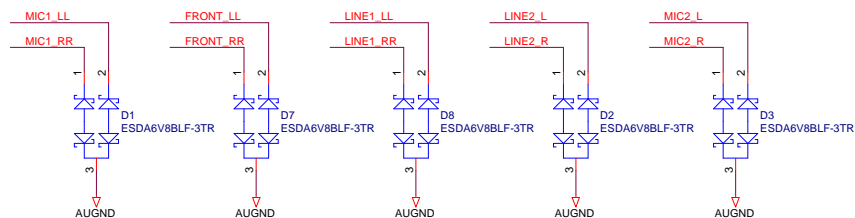
ALC662-VD0-GRS
PN: 01-278-662350



Elitegroup Computer Systems			
Title	AUDIO-ALC662_VD		
Size	Custom	Document Number	Q27H4-AD
Date:	Tuesday, January 03, 2017	Sheet	33 of 47
		Rev	V1.0

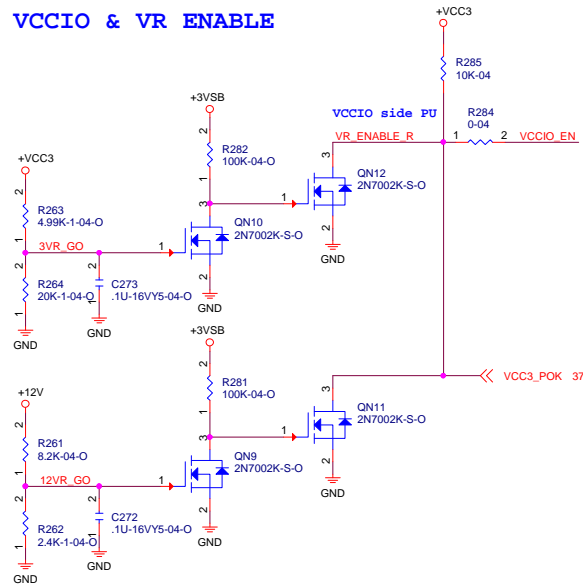


A	B	C
1	2	3
4	5	6
7	8	9
10	11	12
13	14	15
16	17	18
19	20	21
22	23	24
25	26	27
28	29	30
31	32	33
34	35	36
37	38	39
40	41	42
43	44	45
46	47	48
49	50	51
52	53	54
55	56	57
58	59	60
61	62	63
64	65	66
67	68	69
70	71	72
73	74	75
76	77	78
79	80	81
82	83	84
85	86	87
88	89	90
91	92	93
94	95	96
97	98	99
100	101	102

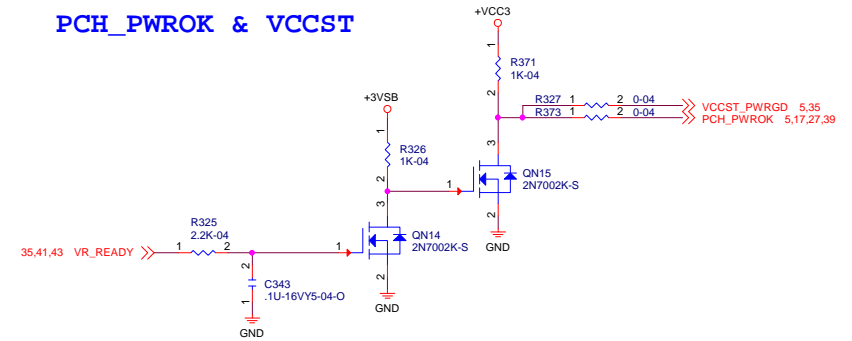


PN:03-100-700872
TVS ARRAY..ESDA6V8BLF-3/TR...SOT-23.5V....LEAD-FREE(RoHS/HF).WILLSEMI

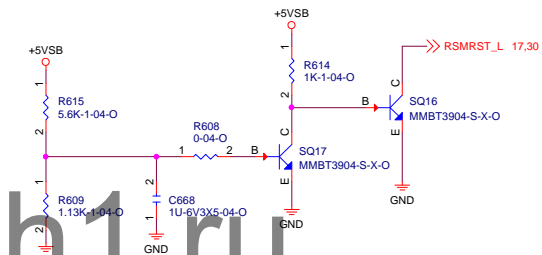
VCCIO & VR ENABLE



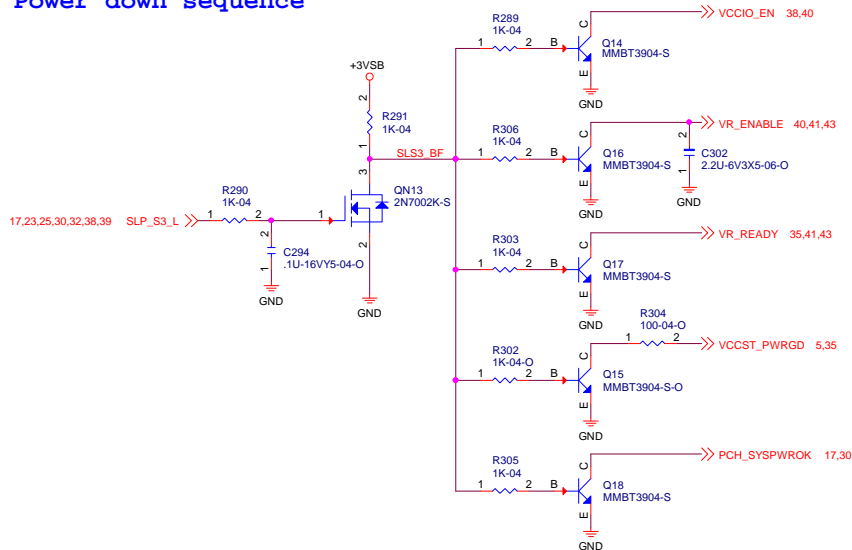
PCH_PWROK & VCCST



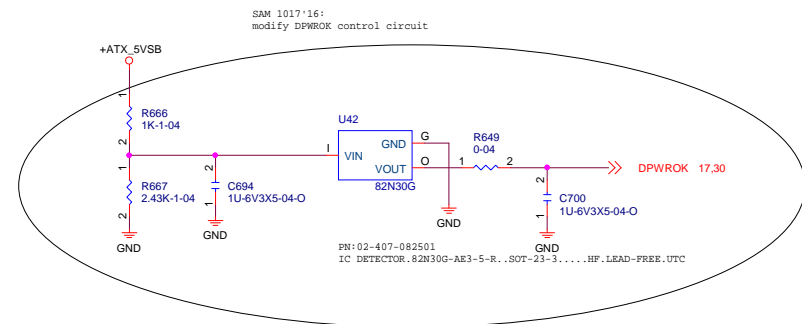
RSMRST#



Power down sequence

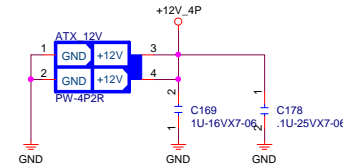
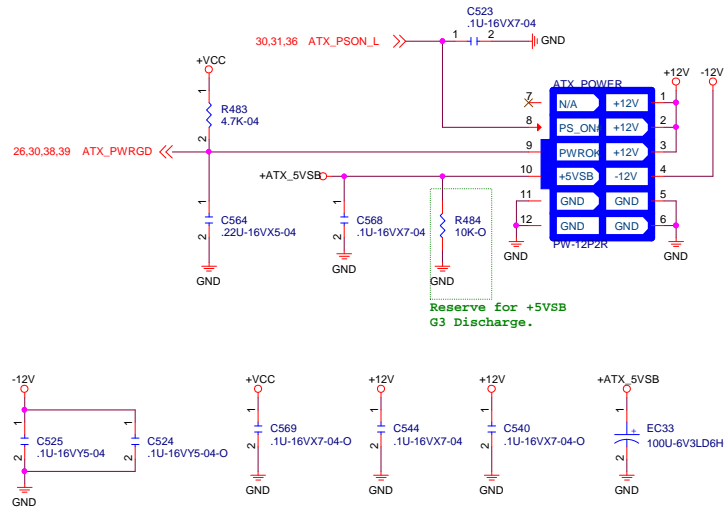


DPWROK

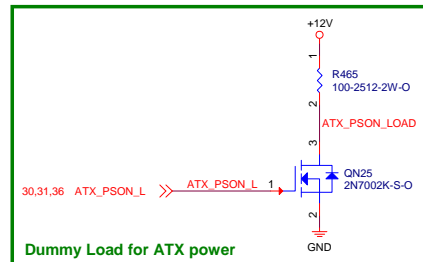
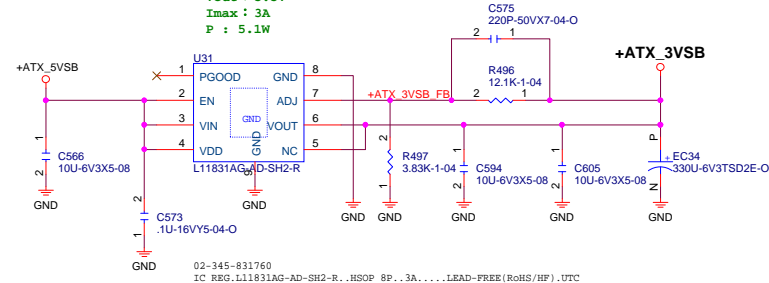


Elitegroup Computer Systems			
Title			
SEQUENCE circuit			
Size	Document Number	Rev	
Custom	Q27H4-AD	V1.0	
Date:	Friday, October 28, 2016	Sheet	35 of 47

www.aitech1.ru

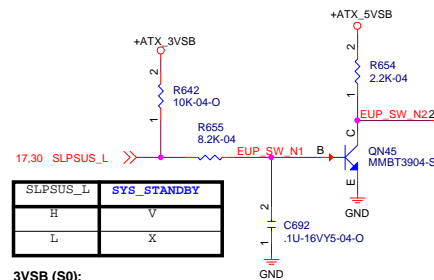


+ATX_3VSB
 Vout : 3.3V
 Imax : 3A
 P : 5.1W



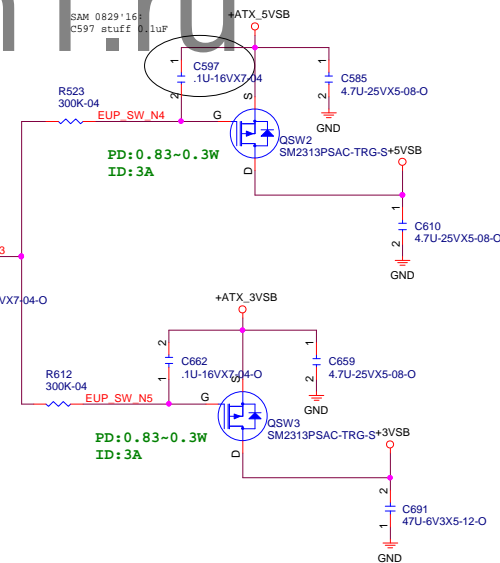
www.aitech1.ru

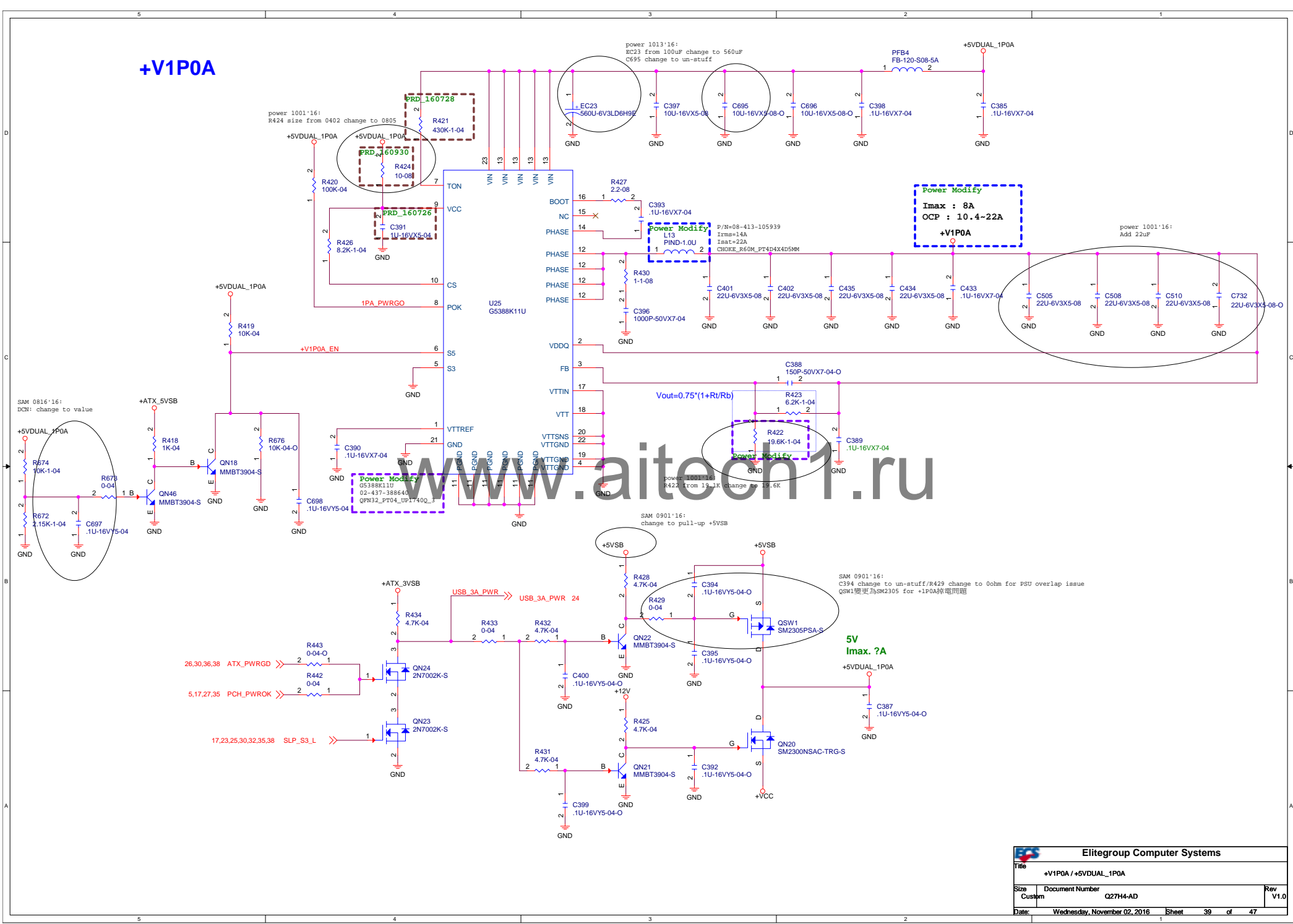
EuP Lot6 Power Saving Circuit



3VSB (S0):

Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A





power 1001'16:
R126 size from 0402 change to 0805

35,41,43 VR_ENABLE << VR_ENABLE

35,38 VCCIO_EN >> VCCIO_EN

Power Modify
G5388K11U
02-437-388640
QWR32_PT04_UP1740Q_3

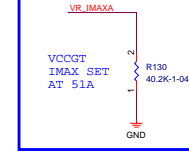
$V_{out} = 0.75 \cdot (1 + R_t/R_b)$

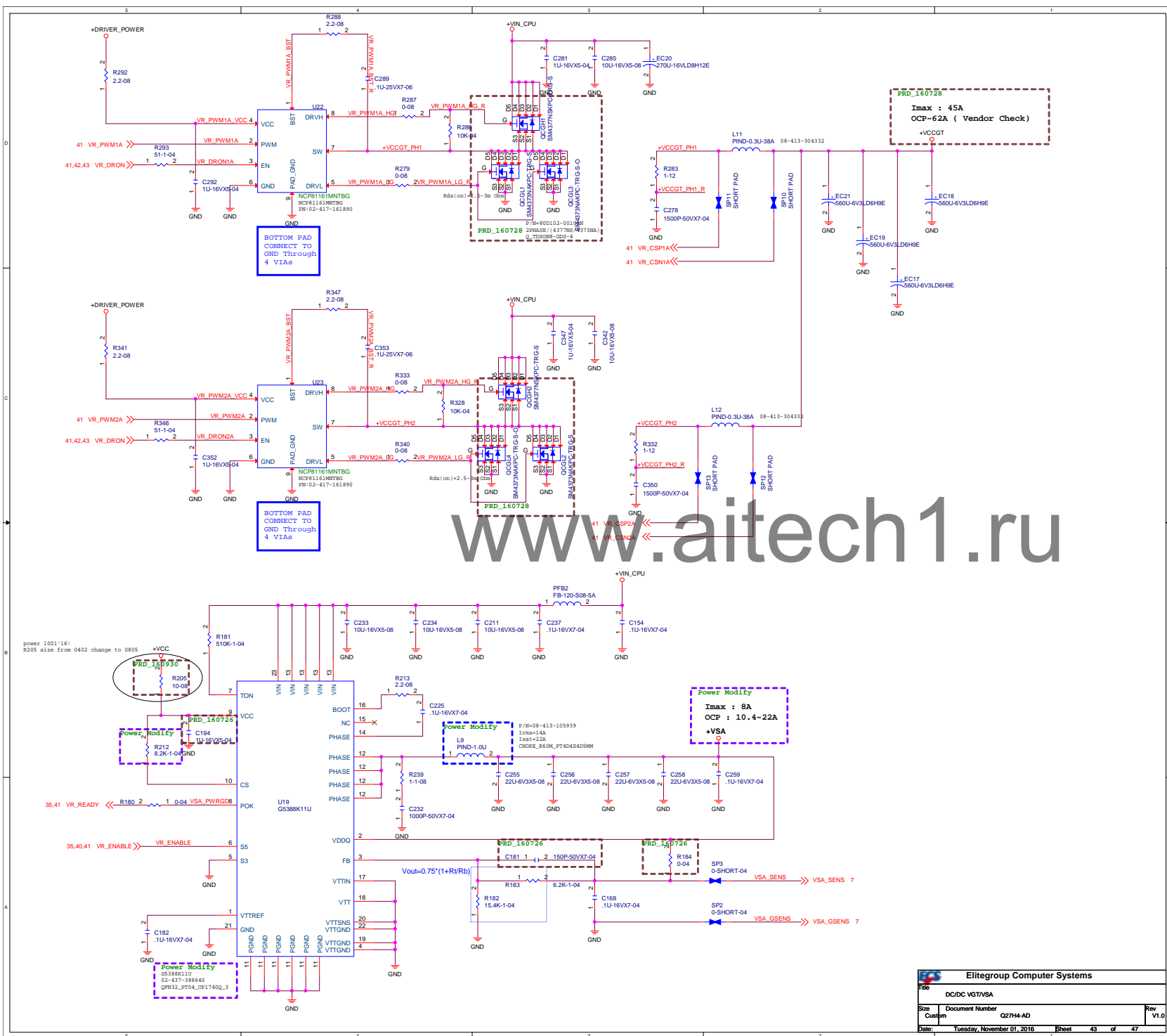
Power Modify
R168
23.2K-1-04

Power Modify
Imax : 5.5A
OCP : 7.2-22A

EE check sequence

Elitegroup Computer Systems			
Title	+VCCIO		
Size	Document Number	Rev	
Custom	Q27H4-AD	V1.0	
Date:	Thursday, November 17, 2016	Sheet	40 of 47





ATX SINGLE P/S		
5VSB +/-5%	12V +/-5%	-12V

ATX4P	
12V +/-5%	



Intel Sky/Kaby Lake CPU			
VCORE	SVID	79A (65W)	
VCC_GT	SVID	45A	
VCC_SA	0.95V	11.1A	
VCCIO	0.95V	5.5A	
VDIMM	1.2V	2.8A	(Iccmax)

DDR4 DIMM	
VDIMM	11A (TDC)
VDIMM_VTT	1A
VPP	2.24A

Intel PCH-H (Q270/B250)			
		S0(A)	Sx(mA)
VCCPRIM_1p0	1V	6.01A	87.4
VCCCLK1	1V	0.035A	0.194
VCCCLK2	1V	0.204A	0.645
VCCCLK3	1V	0.057A	0.22
VCCCLK4	1V	0.036A	0.363
VCCCLK5	1V	0.01A	1.38
VCCMPHY_1p0	1V	3	4
VCCHDAPLL_1p0	1V	0.033A	0.481
VCCAMPHYPLL_1p0	1V	0.08A	0.55
VCCAPLLEBB_1p0	1V	0.075A	0.15
VCCMIPIPLL_1p0	1V	0.036A	0.2
VCCUSB2PLL_1p0	1V	0.012A	0.983
VCCPGPPA	3.3V	0.082A	1.47
VCCPGPPBCH	3.3V	0.229A	0.92
VCCPGPPD	3.3V	0.078A	0.93
VCCPGPEF	3.3V	0.114A	0.6
VCCPGPPG	3.3V	0.065A	0.624
VCCSPI	3.3V	0.029A	0.432
VCCATS	3.3V	0.007A	0.158
VCCHDA	3.3V	0.075A	0.05
VCCPRIM_3p3	3.3V	0.171A	0.543
VCCDSW_3p3	3.3V	0.204A	3.41
VCCRTCPRIM_3p3	3.3V	0.35mA	0.227
VCCRTC	3.0V	0.35mA	0.065

table 10-6

www.aitech1.ru

Icc (mA)	Details
700	All HSIO disabled. Assumes DM1 x4 Running 100%.
132	Each USB 3.0 Port
154	Each PCIe Gen3 Lane
54	First SATA Gen3 Port
132	Each Additional SATA Gen3 Port
102	Each PCIe Gen2 Lane
44	GPIO Port

3VDUAL	
+3VSB	+VCC3

M.2 Slot per key E	
wireless	
VCC3 2A(S0)	3VSB

Total 1 Slots

FAN			
CPU_FAN	+12V	1A	
SYS_FAN	+12V	1A	

X16 PCIe Slot per			
3.3V	3A(S0)		
12V	5.5A(S0)		
3.3Vaux	0.375A		

Total 1 Slot

X1 PCIe Slot per			
3.3V	3A(S0)		
12V	0.5A(S0)		
3.3Vaux	0.375A		

Total 1 Slots

SATA power per			
12V	1A		
5V	1A		

Total 2 connector

front USB3.0 power switch GS7607SO-RS			
each USB3.0	5VDual	0.9A	
PS/2	5VDual	275mA	

Total 4 port

front USB3.0 power switch GS7615STDK-R			
each USB3.0	5VDual	1.5A+0.9A	

Total 2 port

USB2.0 power switch GS7605ST-RS			
each USB2.0	5VDual	0.5A	

Total 5 port

LAN Jacksonville I219LM			
VDD3P3	3.3V	164mA	

AUDIO ALC662-VD			
DVDD 3.3V	3.3V	11mA	
AVDD	5V	42mA	

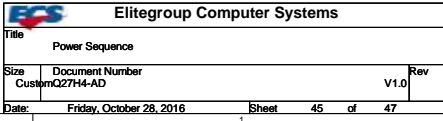
Internal LDO

SIO IT8733			
3VSB	3.3V	14mA	
VCC3	3.3V	TBD	
VBAT	3.3V	2uA	

LAN RTL8111EPV			
VDD3P3	3.3V	270mA	

Elitegroup Computer Systems			
Title	Power Delivery		
Size	Custom	Document Number	Q27H4-AD
Date:	Monday, December 19, 2016	Sheet	44 of 47

Rev V1.0



History

Rev	Date	Notes
A	0901	01.CPU steel's reference from "CPU1" change to "CPU"(P08) 02.F1's footprint change to 0805 & BOM keep using 0805 fuse(P14) 03.wrong net name: change net name to "DONGLE_DP2" on QN4 pin G(P14) 04.SR97 change to stuff 2-3pin, R417 open ME_DISABLE header/jumper change to un-stuff for ME diasable by SW(P17) 05.un-stuff ME_TEST header(P17) 06.R406 stuffed 33ohm for debug card display(P19) 07.C674 change to open & R611 change to 0ohm & R628 change to pull-up +5VSB. U38 use GS7615STDK / G517G1TO1U(P24) 08.stuffed SBOSS1/SBOSS2 for M2_2 holder(P26) 09.C597 stuffed 0.1uF(P36) 10.C713/C721 stuffed 4.7uF(P37) 11.change R485 connection & stuff 10Kohm(P38) 12.C394 change to un-stuff & R429 change to 0ohm & R428 change to pull-up +5VSB(P39) 13.Z1/SZ1 change to use SHORT PAD footprint(P42) 14.For VGA H/Vsync undershoot issue, the damping is changed to 47ohm(P16)
	1001	power change item: 1.C717/C707/C710/C712 change to use 6.3V R690 from 261K change to 200K R693 from 182K change to 150K(P37) 2.R549變更為0805用料,R520 change to 9.53K(P38) 3.R424變更為0805用料,R422變更為19.6K ADD C505/C508/C510 22uF MLCC(P39) 4.R126變更為0805用料(P40) 5.R205變更為0805用料(P43)
	1003	1.SPEC change: DVI-D change to HDMI(P15) 2.SPEC change: power on by monitor (P30)

www.aitech1.ru

